What Is Claimed Is:

1. An electrostatic discharge protection device is located between a pad and an internal circuit, and is coupled to a first level signal and a second level signal, comprising:

a device for detecting the voltage level of the first level signal, wherein when the voltage level of the first level signal reaches a first predetermined value, the voltage detecting device outputs a detecting result signal;

a signal converting device for outputting the second level signal when the detected result signal is recieved;

a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch has a first controlling gate and turns on when the voltage level of the pad reaches a second predetermined voltage level;

a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch has a second controlling gate and turns on and raises the voltage value of the first level signal when the voltage level of the pad reaches a third predetermined voltage level; and

a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch has a third controlling gate and turns on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the second level signal.

2. The electrostatic discharge protection device as claimed in claim 1, wherein the first switch and the third switch are NMOS transistors.

3. The electrostatic discharge protection device as claimed in claim 2, wherein the second switch is a PMOS transistor.

4. The electrostatic discharge protection device as claimed in claim 3, wherein the voltage detecting device comprises at least one serial diode, and turn-on voltage of the serial diodes is between the first level signal and the first predetermined voltage level.

5. The electrostatic discharge protection device as claimed in claim 4, wherein the signal converting device comprises:

a switching circuit coupled to the voltage detecting device, wherein the switching circuit outputs a ground level enable signal when receiving the detecting result signal; and

a driving circuit coupled to the switching circuit, the driving circuit outputs the second level signal when receiving the ground level enable signal.

6. The electrostatic discharge protection device as claimed in claim 5, wherein the first level signal is a power source signal.

7. The electrostatic discharge protection device as claimed in claim 6, wherein the second level signal is ground level.

8. The electrostatic discharge protection device as claimed in claim 7, wherein the second predetermined voltage level is a break down voltage of the NMOS transistor.

9. The electrostatic discharge protection device as claimed in claim 8, wherein the third predetermined voltage level is a

voltage difference to make the PMOS transistor generate leakage current.

10. The electrostatic discharge protection device as claimed in claim 5, wherein the first controlling gate, the second controlling gate, and the third controlling gate are gates of a MOS transistor.

11. An electrostatic discharge protection device located between a pad and an internal circuit, and is coupled to a first level signal, a second level signal, and a third level signal, comprising:

a voltage detecting device for detecting the voltage level of the third level signal, wherein when the voltage level of the third level signal reaches a first predetermined value, the voltage detecting device outputs a detecting result signal;

a switching circuit coupled to the voltage detecting device, the switching circuit outputs a ground level enable signal when receiving the detecting result signal;

a driving circuit coupled to the switching circuit and the voltage detecting device for generating the third level signal, wherein the driving circuit outputs the second level signal when receiving the ground level enable signal;

a first switch coupled to a connection point between the pad and the internal circuit, wherein the first switch has a first controlling gate and turns on when the voltage level of the pad reaches a second predetermined voltage level;

a second switch coupled to the connection point between the pad and the internal circuit, wherein the second switch has a

second controlling gate and turns on and raises the voltage value of the first level signal when the voltage level of the pad reaches a third predetermined voltage level; and

a third switch coupled to the connection point between the pad and the internal circuit, wherein the third switch has a third controlling gate and turns on when the voltage level of the pad reaches the second predetermined voltage level and the third controlling gate receives the second level signal.

12. The electrostatic discharge protection device as claimed in claim 11, wherein the first switch and the third switch are NMOS transistors.

13. The electrostatic discharge protection device as claimed in claim 12, wherein the second switch is a PMOS transistor.

14. The electrostatic discharge protection device as claimed in claim 13, wherein the voltage detecting device comprises at least one serial diode, and turn-on voltage of the serial diodes is between the third level signal and the first predetermined voltage level.

15. The electrostatic discharge protection device as claimed in claim 14, wherein the first level signal is power source signal.

16. The electrostatic discharge protection device as claimed in claim 15, wherein the second level signal is in ground level.

17. The electrostatic discharge protection device as claimed in claim 16, wherein the second predetermined voltage level is a break down voltage of the NMOS transistor.

18. The electrostatic discharge protection device as claimed in claim 17, wherein the third predetermined voltage level is a voltage difference to make the PMOS transistor generate leakage current.

19. The electrostatic discharge protection device as claimed in claim 18, wherein the first controlling gate, the second controlling gate, and the third controlling gate are gates of a MOS transistor.